WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first and a second bit line in a first region and connected to a plurality of memory cells;

an offset-compensated amplifier circuit structured to detect a voltage variation of the first bit line based on a reference voltage and to drive the second bit line according to a detection result; and

a sense amplifier circuit in a second region and structured to sense and amplify a voltage difference between the first and second bit lines,

wherein the offset-compensated amplifier circuit is structured to compensate an offset voltage with respect to the reference voltage in response to a first control signal before the voltage variation of the first bit line is detected; and wherein a part of the offset-compensated amplifier circuit is disposed at the first region and a remaining part of the offset-compensated amplifier circuit is disposed at a third region that is different from the first and second regions.

2. The semiconductor memory device according to claim 1, wherein the offset-compensated amplifier circuit is structured to operate before row activation.

3. The semiconductor memory device according to claim 1, wherein the offset-compensated amplifier circuit is structured to be inactivated before activation of the sense amplifier circuit.

4. The semiconductor memory device according to claim 1, wherein the offset-compensated amplifier circuit is structured to be inactivated after activation of the sense amplifier circuit.

5. The semiconductor memory device according to claim 1, wherein the offset-compensated amplifier circuit comprises:

a differential amplifier having a first input terminal connected to the first bit line, a second input terminal connected to receive the reference voltage, and an output terminal connected to the second bit line; and

a switch that is connected between the output terminal and the first input terminal and is structured to operate responsive to the first control signal.

6. The semiconductor memory device according to claim 1, wherein the offset-compensated amplifier circuit comprises:

a first means that operates responsive to a second control signal and is structured to generate a bias voltage according to the reference voltage;

a second means that is supplied with the bias voltage and is structured to establish a voltage of the second bit line in response to the voltage variation of the first bit line; and

a switch that is connected between the first and second bit lines and is structured to operate responsive to the first control signal.

7. The semiconductor memory device according to claim 6, wherein the switch and the second means are in the second region, and the first means is in the third region.

8. The semiconductor memory device according to claim 7, wherein drivers for driving the sense amplifier circuit are located in the third region.

9. The semiconductor memory device according to claim 6, wherein the reference voltage is equal to a bit line precharge voltage.

10. The semiconductor memory device according to claim 6, wherein the reference voltage is greater than a bit line precharge voltage.

11. The semiconductor memory device according to claim 6, wherein the first means comprises:

a first transistor that has a current path formed between a power supply voltage a first internal node configured to output the bias voltage, and has a gate connected to the first internal node;

a second transistor that has a current path between the first internal node and a second internal node, and has a gate configured to receive the reference voltage; and

a third transistor that has a current path formed between the second internal node a ground voltage, and has a gate configured to receive the second control signal.

12. The semiconductor memory device according to claim 11, wherein the first means further comprises a fourth transistor that has a current path formed between the power supply voltage and the first internal node, and has a gate configured to receive the second control signal.

13. The semiconductor memory device according to claim 12, wherein the second means comprises:

a fifth transistor that has a current path formed between the power supply voltage and the second bit line, and has a gate connected to receive the bias voltage; and

a sixth transistor that has a current path formed between the output terminal and the second internal node, and has a gate connected to the one bit line.

14. The semiconductor memory device according to claim 5, further comprising a gate circuit that operates responsive to a first gate signal and a second gate signal, and that is connected between the first and second bit lines and the differential amplifier.

15. The semiconductor memory device according to claim 14, wherein the gate circuit connects the first bit line to the first input terminal of the differential amplifier and connects the second bit line to the output terminal of the differential amplifier in response to the first and second gate signals, respectively, the second input terminal of the differential amplifier being structured to be supplied with the reference voltage.

16. The semiconductor memory device according to claim 14, wherein the gate circuit connects the second bit line to the first input terminal of the differential amplifier and connects the first bit line to the output terminal of the differential amplifier in response to the first and second gate signals, respectively.

17. The semiconductor memory device according to claim 12, wherein the second means comprises:

a fifth transistor that has a current path formed between the power supply voltage and the second bit line, and has a gate connected to the second internal node;

a sixth transistor that has a current path formed between the second bit line and a third internal node, and has a gate connected to the first bit line; and

a seventh transistor that has a current path formed between the third internal node and the ground voltage, and has a gate configured to receive the second control signal.

18. A semiconductor memory device comprising:

a first and a second bit line in a first region and connected to a plurality of memory cells;

a bias voltage generator circuit that operates responsive to a first control signal and is structured to generate a bias voltage based on a reference voltage;

a driver circuit structured to be supplied with the bias voltage and structured to drive the second bit line in response to voltage variation of the first bit line;

a switch structured to electrically connect the first and second bit lines in response to a second control signal; and

a sense amplifier circuit in a second region and structured to sense and amplify a voltage difference between the first and second bit lines,

wherein the bias voltage generator circuit and the driver circuit form a differential amplifier; and wherein the driver circuit and the switch are disposed at the second region and the bias voltage generator circuit is disposed at a third region different from the first and second regions.

19. The semiconductor memory device according to claim 18, wherein the first control signal is structured to be activated before row activation and inactivated before activation of the sense amplifier circuit.

20. The semiconductor memory device according to claim 18, wherein the first control signal is structured to be activated before row activation and inactivated after activation of the sense amplifier circuit.

21. The semiconductor memory device according to claim 18, wherein the second control signal is structured to be activated during a predetermined time before row activation.

22. The semiconductor memory device according to claim 18, wherein the bias voltage generator circuit comprises:

a first transistor that has a current path formed between a power supply voltage a first internal node configured to output the bias voltage, and has a gate connected to the first internal node;

a second transistor that has a current path formed between the first internal node and a second node and has a gate connected to receive the reference voltage;

a third transistor that has a current path formed between the second internal node and a ground voltage, and has a gate connected to receive the first control signal; and

a fourth transistor that has a current path formed between the power supply voltage and the first internal node and has a gate connected to receive the first control signal.

23. The semiconductor memory device according to claim 22, wherein the driver circuit comprises:

a fifth transistor that has a current path formed between the power supply voltage and the second bit line, and has a gate connected to the first internal node; and

a sixth transistor that has a current path formed between the second bit line and the second internal node, and has a gate connected to the first bit line.

24. The semiconductor memory device according to claim 22, wherein the driver circuit comprises:

a fifth transistor that has a current path formed between the power supply voltage and the second bit line, and has a gate connected to the second internal node;

a sixth transistor that has a current path formed between the second bit line and a third internal node, and has a gate connected to the first bit line; and

a seventh transistor that has a current path formed between the third internal node and the ground voltage, and has a gate connected to the second control signal.

25. The semiconductor memory device according to claim 18, wherein when the first and second control signals are activated, a negative feedback loop is formed at the differential amplifier via the switch, so that an input offset voltage of the differential amplifier is removed.

26. The semiconductor memory device according to claim 25, wherein the driver circuit drives the second bit line in response to voltage variation of the first bit line, after the input offset voltage of the differential amplifier is removed.

27. A semiconductor memory device comprising:

first, second, third, and fourth bit lines that are in a first region and connected to a plurality of memory cells ;

a bias voltage generator circuit that operates responsive to a first control signal and generates a bias voltage based on a reference voltage;

a first driver circuit that is supplied with the bias voltage and drives the second bit line in response to voltage variation of the first bit line;

a second driver circuit that is supplied with the bias voltage and drives the fourth bit line in response to voltage variation of the third bit line;

a first switch circuit that electrically connects the first and second bit lines in response to a second control signal;

a second switch circuit that electrically connects the third and fourth bit lines in response to the second control signal;

a third switch circuit that provides the first and second driver circuits with a discharge path in response to the first control signal, respectively; and

a sense amplifier circuit that is placed at a second region and senses and amplifies a voltage difference between the first and second bit lines and a voltage difference between the third and fourth bit lines, respectively,

wherein the bias voltage generator circuit, the first driver circuit, and the third switch circuit form a first differential amplifier, and the bias voltage generator circuit, the second driver circuit, and the third switch circuit form a second differential amplifier; and

wherein the first and second driver circuits and the first to third switch circuits are in the second region, and the bias voltage generator circuit is located in a third region that is different from the first and second regions.

28. The semiconductor memory device according to claim 27, wherein the first driver circuit comprises:

a first transistor that has a current path formed between a power supply voltage and the second bit line, and has a gate connected to receive the bias voltage; and

a second transistor that has a current path formed between the second bit line and the third switch circuit, and has a gate connected to the first bit line.

29. The semiconductor memory device according to claim 27, wherein the second driver circuit comprises:

a first transistor that has a current path formed between a power supply voltage and the second bit line, and has a gate connected to receive the bias voltage; and

a second transistor that has a current path formed between the second bit line and the third switch circuit, and has a gate connected to the first bit line.

30. The semiconductor memory device according to claim 27, further comprising:

a first gate circuit that operates responsive to first and second gate signals, and is connected between the first and second bit lines and the first differential amplifier; and

a second gate circuit that operates responsive to the first and second gate signals, and is connected between the third and fourth bit lines and the second differential amplifier.

31. The semiconductor memory device according to claim 30, wherein the first differential amplifier has a first input terminal connected to the first bit line, a second input terminal supplied with the reference voltage, and an output terminal connected to the second bit line.

32. The semiconductor memory device according to claim 31, wherein the first gate circuit connects the first bit line to the first input terminal of the first differential amplifier and the second bit line to the output terminal of the first differential amplifier, in response to the first and second signals.

33. The semiconductor memory device according to claim 30, wherein the second differential amplifier has a first input terminal connected to the third bit line, a second input terminal supplied with the reference voltage, and an output terminal connected to the fourth bit line.

34. The semiconductor memory device according to claim 33, wherein the first gate circuit connects the third bit line to the first input terminal of the first differential amplifier and connects the fourth bit line to the output terminal of the first differential amplifier, in response to the first and second signals.

35. The semiconductor memory device according to claim 33, wherein the first gate circuit connects the fourth bit line to the first input terminal of the first differential amplifier and connects the third bit line to the output terminal of the first differential amplifier, in response to the first and second signals.

36. The semiconductor memory device according to claim 27, wherein when the first and second control signals are activated a negative feedback loop is formed at the first differential amplifier via the first switch circuit, so that an input offset voltage of the first differential amplifier is removed.

37. The semiconductor memory device according to claim 36, wherein the first driver circuit drives the second bit line in response to voltage variation of the first bit line, after the input offset voltage of the first differential amplifier is removed.

38. The semiconductor memory device according to claim 27, wherein when the first and second control signals are activated a negative feedback loop is formed at the second differential amplifier via the second switch circuit, so that an input offset voltage of the second differential amplifier is removed.

39. The semiconductor memory device according to claim 38, wherein the second driver circuit drives the fourth bit line in response to voltage variation of the third bit line, after the input offset voltage of the second differential amplifier is removed.

40. A semiconductor memory device comprising:

a first and a second bit line, each of which connected to a plurality of memory cells in a first region;

a first bias voltage generator circuit which operates responsive to a first control signal and generates a first bias voltage based on a reference voltage;

a second bias voltage generator circuit which operates responsive to a second control signal and generates a second bias voltage based on the reference voltage;

a first driver circuit which is supplied with the first bias voltage and drives the second bit line in response to voltage variation of the first bit line;

a second driver circuit which is supplied with the second bias voltage and drives the first bit line in response to voltage variation of the second bit line;

a switch circuit which electrically connects the first and second bit lines in response to a third control signal; and

a sense amplifier circuit which is disposed at a second region and senses and amplifies a voltage difference between the first and second bit lines,

wherein the first bias voltage generator circuit and the first driver circuit form a first differential amplifier, and the second bias voltage generator circuit and the second driver circuit form a second differential amplifier; and

wherein the first and second driver circuits and the switch circuit are located in the second region, and the first and second bias voltage generator circuits are located in a third region that is disposed at a different place from the first and second regions.

41. The semiconductor memory device according to claim 40, wherein a plurality of drivers configured to drive the sense amplifier are located in the third region.

42. The semiconductor memory device according to claim 40, wherein the first and second control signals are complementary signals.

43. The semiconductor memory device according to claim 40, wherein the first and second control signals are activated respectively before row activation and inactivated either before or after activation of the sense amplifier circuit.

44. The semiconductor memory device according to claim 40, wherein the third control signal is activated during a predetermined time before row activation.

45. The semiconductor memory device according to claim 40, wherein when the first and third control signals are activated, a negative feedback loop is formed at the first differential amplifier via the switch circuit, so that an input offset voltage of the first differential amplifier is removed.

46. The semiconductor memory device according to claim 40, wherein the first driver circuit drives the second bit line in response to voltage variation of the first bit line, after the input offset voltage of the first differential amplifier is removed.

47. The semiconductor memory device according to claim 40, wherein when the second and third control signals are activated a negative feedback loop is formed at the second differential amplifier via the switch circuit, so that an input offset voltage of the second differential amplifier is removed.

48. The semiconductor memory device according to claim 47, wherein the second driver circuit drives the first bit line in response to voltage variation of the second bit line, after the input offset voltage of the second differential amplifier is removed.

49. A semiconductor memory device comprising:

first, second, third, and fourth bit lines each of which is connected to a plurality of memory cells disposed at a first region;

a first bias voltage generator circuit that operates responsive to a first control signal and generates a first bias voltage based on a reference voltage;

a second bias voltage generator circuit that operates responsive to a second control signal and generates a second bias voltage based on the reference voltage;

a first driver circuit that is supplied with the first bias voltage and drives the second bit line in response to voltage variation of the first bit line;

a second driver circuit that is supplied with the first bias voltage and drives the fourth bit line in response to voltage variation of the third bit line;

a first switch circuit that electrically connects the first and second bit lines in response to a third control signal;

a second switch circuit that electrically connects the third and fourth bit lines in response to the third control signal;

a third switch circuit that provides a discharge path to the first driver circuit in response to the first control signal;

a fourth switch circuit that provides a discharge path to the second driver circuit in response to the second control signal; and

a sense amplifier circuit that is located in a second region and senses and amplifies voltage differences between the first and second bit lines and between the third and fourth bit lines, respectively,

wherein the first bias voltage generator circuit, the first driver circuit, and the third switch circuit form a first differential amplifier, and the second bias voltage generator circuit,

the second driver circuit, and the fourth switch circuit form a second differential amplifier; and

wherein the first and second driver circuits and the first to fourth switch circuits are located in the second region, and the first and second bias voltage generator circuits are located in a third region that is different from the first and second regions.

50. The semiconductor memory device according to claim 49, wherein drivers for driving the sense amplifier are located in the third region.

51. The semiconductor memory device according to claim 49, wherein the first and second control signals are complementary signals.

52. The semiconductor memory device according to claim 51, wherein the first and second control signals are activated before row activation and inactivated either before or after activation of the sense amplifier.

53. The semiconductor memory device according to claim 49, wherein the third control signal is activated during a predetermined time before row activation.

54. The semiconductor memory device according to claim 49, wherein when the first and third control signals are activated, a negative feedback loop is formed at the first differential amplifier via the first switch circuit, so that an input offset voltage of the first differential amplifier is removed.

55. The semiconductor memory device according to claim 54, wherein the first driver circuit drives the second bit line in response to voltage variation of the first bit line, after the input offset voltage of the first differential amplifier is removed.

56. The semiconductor memory device according to claim 49, wherein when the second and third control signals are activated a negative feedback loop is formed at the second differential amplifier via the second switch circuit, so that an input offset voltage of the second differential amplifier is removed.

57. The semiconductor memory device according to claim 56, wherein the second driver circuit drives the first bit line in response to voltage variation of the second bit line, after the input offset voltage of the second differential amplifier is removed.